CLAIMS

Having thus described our invention in detail, what we claim as new and desire to secure by the Letters Patent is:

1. A planar hybrid-orientation semiconductor-on-insulator (SOI) substrate structure comprising:

at least two clearly defined single crystal semiconductor regions with different surface orientations, said at least two clearly defined single crystal semiconductor regions disposed on a common buried insulating layer, said common buried insulating layer disposed on a substrate.

2. The planar hybrid-orientation SOI substrate structure of Claim 1 further comprising at least one isolation region separating said at least two clearly defined single crystal semiconductor regions from each other.

3. The planar hybrid-orientation SOI substrate structure of Claim 2 wherein said at least one isolation region is a trench isolation region.

4. The planar hybrid-orientation SOI substrate structure of Claim 2 wherein said at least one isolation region extends down to at least an upper surface of the common buried insulating layer.

5. The planar hybrid-orientation SOI substrate structure of Claim 2 wherein said at least one isolation region does not extend down to said common buried insulating layer.

6. The planar hybrid-orientation SOI substrate structure of Claim 1 wherein said at least two clearly defined single crystal semiconductor regions comprise the same or different semiconductor materials.

7. The planar hybrid-orientation SOI substrate structure of Claim 6 wherein said semiconductor materials are selected from the group consisting of Si, SiC, SiGe, SiGeC, Ge alloys, Ge, C, GaAs, InAs, InP, layered combinations or alloys thereof, and other III-V or II-VI compound semiconductors.

8. The planar hybrid-orientation SOI substrate structure of Claim 1 wherein said at least two clearly defined single crystal semiconductor regions with different surface orientations both comprise a Si-containing semiconductor material.

9. The planar hybrid-orientation SOI substrate structure of Claim 1 wherein said at least two clearly defined single crystal semiconductor regions are each comprised of strained, unstrained or a combination of strained and unstrained semiconductor materials.

10. The planar hybrid-orientation SOI substrate structure of Claim 1 wherein said different surface orientations are selected from the group consisting of (110), (111) and (100).

11. The planar hybrid-orientation SOI substrate structure of Claim 8 wherein said different surface orientations are selected from the group consisting of (110), (111) and (100).

12. The planar hybrid-orientation SOI substrate structure of Claim 11 wherein said first Si-containing semiconductor region has a (100) crystal orientation and said second Si-containing semiconductor region has a (110) crystal orientation.

13. The planar hybrid-orientation SOI substrate structure of Claim 12 further comprising at least one nFET device and at least one pFET device, wherein said at least one nFET device is located on said (100) crystal orientation and said at least pFET device is located on said (110) crystal orientation.

14. The planar hybrid-orientation SOI substrate structure of Claim 1 further comprising at least one nFET device and at least one pFET device, wherein said at least one nFET device is located on a crystal orientation that is optimal for said device said at least pFET device is located on a crystal orientation that is optimal for said device.

15. The planar hybrid-orientation SOI substrate structure of Claim 1 wherein said buried insulating layer is a dielectric material selected from the group consisting of SiO_2, crystalline SiO_2, SiO_2 containing nitrogen, silicon nitride, metal oxides, metal nitrides, and highly thermally conductive materials.

16. The planar hybrid-orientation SOI substrate structure of Claim 15 wherein said dielectric material is SiO_2 or crystalline SiO_2.

17. The planar hybrid-orientation SOI substrate structure of Claim 1 wherein said substrate is a semiconductor material selected from the group consisting of Si, SiC, SiGe, SiGeC, Ge alloys, Ge, C, GaAs, InAs, InP, layered combinations or alloys thereof, and other III-V or II-VI compound semiconductors.

18. The planar hybrid-orientation SOI substrate structure of Claim 1 wherein said substrate has an epitiaxial relationship to at least one of said single crystal semiconductor regions.

19. The planar hybrid-orientation SOI substrate structure of Claim 1 wherein said at least two clearly defined single crystal semiconductor regions comprise three single crystal semiconductor regions of different crystal orientation that are separated by isolation regions.

20. The planar-hybrid-orientation SOI substrate structure of Claim 19 further comprising at least one nFET device and at least one pFET device, wherein said at least one nFET device is located on a crystal orientation that is optimal for said device said at least pFET device is located on a crystal orientation that is optimal for said device.

21. The planar-hybrid-orientation SOI substrate structure of Claim 1 wherein at least one of said at least two clearly defined single crystal regions comprises an upper semiconductor disposed on a lower, residual semiconductor, said upper and lower semiconductors having different surface orientations, said residual semiconductor in direct contact with said common buried insulating layer.

22. The planar-hybrid-orientation SOI substrate structure of Claim 21 further comprising at least one nFET device and at least one pFET device, wherein said at least one nFET device is located on a crystal orientation that is optimal for said device said at least pFET device is located on a crystal orientation that is optimal for said device.

23. The planar hybrid-orientation SOI substrate structure of Claim 21 further comprising at least one isolation region separating said at least two clearly defined single

crystal semiconductor regions from each other, wherein said at least one isolation region extends down at least to said common buried insulating layer.

24. The planar hybrid-orientation SOI substrate structure of Claim 21 further comprising at least one isolation region separating said at least two clearly defined single crystal semiconductor regions from each other, wherein said at least one isolation region does not extend down to said common buried insulating layer.

25. The planar hybrid-orientation SOI substrate structure of Claim 1 wherein said substrate is an insulator.

26. The planar hybrid-orientation SOI substrate structure of Claim 8 wherein at least one of said at least two clearly defined single crystal Si-containing semiconductor regions comprises an upper Si-containing semiconductor disposed on a lower, residual Si-containing semiconductor, said upper and lower semiconductors having different surface orientations, said residual semiconductor in direct contact with said common buried oxide layer.

27. The planar hybrid-orientation SOI substrate structure of Claim 26 wherein said different surface orientations are selected from the group consisting of (110), (111) and (100).

28. The planar hybrid-orientation SOI substrate structure of Claim 27 wherein first Si-containing semiconductor region has a (100) crystal orientation and said second Si-containing semiconductor region has a (110) crystal orientation.

29. The planar hybrid-orientation SOI substrate structure of Claim 28 further comprising at least one nFET device and at least one pFET device, wherein said at least one nFET device is located on said (100) crystal orientation and said at least pFET device is located on said (110) crystal orientation.

30. The planar hybrid-orientation SOI substrate structure of Claim 26 further comprising at least one nFET device and at least one pFET device, wherein said at least one nFET device is located on a crystal orientation that is optimal for said device said at least pFET device is located on a crystal orientation that is optimal for said device.

31. The planar hybrid-orientation SOI substrate structure of Claim 26 further comprising at least one isolation region separating said at least two clearly defined single crystal Si-containing semiconductor regions from each other.

32. The planar hybrid-orientation SOI substrate structure of Claim 31 wherein said at least one isolation region is a trench isolation region.

33. The planar hybrid-orientation SOI substrate structure of Claim 31 wherein said at least one isolation region extends down to at least an upper surface of the common buried insulating layer.

34. The planar hybrid-orientation SOI substrate structure of Claim 31 wherein said at least one isolation region does not extend to said common buried oxide layer.

35. A method of forming a planar hybrid-orientation substrate comprising the steps of

forming a bilayer template layer stack comprising a first, lower single crystal semiconductor layer having a first orientation and a second, upper single crystal semiconductor layer having a second orientation different from the first;

amorphizing one of the semiconductor layers of the bilayer template stack in selected areas to form localized amorphized regions; and

recrystallizing the localized amorphized regions using a non-amorphized semiconductor layer of the stack as a template, thereby changing the orientation in the localized amorphized regions from an original orientation to a desired orientation.

36. The method of Claim 35 wherein said first, lower single crystal semiconductor layer is disposed on the insulating layer of an SOI substrate.

37. The method of Claim 35 wherein said first, lower single crystal semiconductor layer comprises a single crystal semiconductor substrate.

38. The method of Claim 35 wherein said second, upper single crystal semiconductor layer is formed atop the first, lower single crystal semiconductor by bonding.

39. The method of Claim 35 wherein said localized amorphized region is formed predominately within the second, upper single crystal semiconductor layer.

40. The method of Claim 35 wherein said localized amorphized region is formed predominately within the first, lower single crystal semiconductor layer.

41. The method of Claim 36 wherein said localized amorphized region is formed predominately within the first, lower single crystal semiconductor layer, and further including the step of removing said top layer after recrystallization, by a process such as chemical mechanical polishing.

42. The method of Claim 35 further comprising forming at least one trench isolation region to separate said areas selected for amorphization from those not selected for amorphization, said at least one trench isolation being formed prior to amorphizing, between amorphizing and recrystallizing, or partially after amorphizing and partially after recrystallizing.

43. The method of Claim 35 wherein said first, lower single crystal semiconductor and layer said second, upper single crystal semiconductor layer are composed of the same or different semiconductor material selected from the group consisting of Si, SiC, SiGe, SiGeC, Ge alloys, Ge, C, GaAs, InAs, InP, layered combinations or alloys thereof, and other III-V or II-VI compound semiconductors.

44. The method of Claim 35 wherein said first, lower single crystal semiconductor layer and said second, upper single crystal semiconductor layer are both composed of a Si-containing semiconductor material.

45. The method of Claim 35 wherein said first, lower single crystal semiconductor layer and said second, upper single crystal semiconductor layer are composed of strained, unstrained or a combination of strained and unstrained semiconductor materials.

46. The method of Claim 35 wherein said first, lower single crystal semiconductor layer and said second, upper single crystal semiconductor layer have different surface orientations selected from (110), (111) and (100).

47. The method of Claim 35 further comprising forming at least one nFET device and at least one pFET device, wherein said at least one nFET device is located on a crystal orientation that is optimal for said device said at least pFET device is located on a crystal orientation that is optimal for said device.

48. The method of Claim 37 further comprising forming a buried insulating layer after said recrystallizing step.

49. The method of Claim 48 wherein said buried insulating layer is formed by a separation-by-ion implantation of oxygen (SIMOX) process.

50. The method of Claim 35 wherein said amorphizing is accomplished by ion implantation.

51. The method of Claim 50 wherein said ion implantation comprises an ion selected from the group consisting of Si, Ge, Ar, C, O, N, H, He, Kr, Xe, P, B and As.

52. The method of Claim 50 wherein said ion implantation comprising an ion selected from the group consisting of Si and Ge.

53. The method of Claim 50 wherein said ion implantation is performed using a patterned mask.

54. The method of Claim 35 wherein said recrystallizing is performed at a temperature from about 200°C to about 1300°C

55. The method of Claim 35 wherein said recrystallizing is performed in a gas selected from the groups consisting of N_2, Ar, He, H_2 and mixtures thereof.